IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant:	Brian N. Ripley	Examiner:	Midys Rojas
Serial No.:	10/091,698	Group Art Unit:	2185
Filed:	March 5, 2002	Docket No.:	100202181-1
Title:	A VARIABLE WIDTH MEMORY SYSTEM AND METHOD		

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This Appeal Brief is submitted in support of the Notice of Appeal filed on October 19, 2009, appealing the final rejection of claims 1-14, 16-20 and 23-25 of the above-identified application as set forth in the Final Office Action mailed July 17, 2009.

The U.S. Patent and Trademark Office is hereby authorized to charge Deposit Account No. 08-2025 in the amount of $510.00 for filing a Brief in Support of an Appeal as set forth under 37 C.F.R. § 41.20(b)(2). At any time during the pendency of this application, please charge any required fees or credit any overpayment to Deposit Account No. 08-2025.

Appellant respectfully requests consideration and reversal of the Examiner's rejection of pending claims 1-14, 16-20 and 23-25.

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REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company, LP having a principal place of business at 11445 Compaq Center Drive West, Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant that will have a bearing on the Board's decision in the present Appeal.

STATUS OF CLAIMS

In a Final Office Action mailed July 17, 2009, claims 1-14, 16-20 and 23-25 were finally rejected. Claims 15, 21 and 22 have been canceled. Claims 1-14, 16-20 and 23-25 are pending in the application and are the subject of the present Appeal.

STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Office Action mailed July 17, 2009.

SUMMARY OF THE CLAIMED SUBJECT MATTER

The following provides a concise explanation of the subject matter defined the independent claims involved in the appeal, referring to the specification by page and line number and to the drawings by reference characters, as required by 37 CFR 41.37(c)(1)(v). Note that the reference to passages in the specification and reference characters in the drawings for each element of the claims does not imply that limitations from the specification and drawings should be read into the corresponding claim element or that these references are the sole sources in the specification and the drawings supporting the claim features.

Independent claim 1 recites a variable width memory system that includes a bus (375) for communicating information. A plurality of single cell variable width memory locations (311) are coupled to the bus. The plurality of single cell variable width memory locations

store information (p. 8, l. 33 – p. 9, l. 8), wherein the plurality of single cell variable width memory locations receive a number of bits corresponding to the width of the single cell variable width memory locations and the width of a variable width register (331) that is located in a processor (330) associated with the variable width memory system. A variable width mapping process provides a correlation between the single cell variable width memory locations and the variable width register (p. 10, ll. 13-18; p. 12, ll. 12-20; p. 14, ll. 6-15). A controller (320) is coupled to the bus, and controller directs access to the plurality of single cell variable width memory locations, wherein the number of bits potentially vary automatically on a per access basis depending on which single cell variable width memory location of the plurality of single cell variable width memory locations is being accessed. All memory locations are not required to have the same width. (p. 13, ll. 14-17)

Independent claim 8 recites a variable width memory mapping method that includes receiving a register indicator corresponding to a register (210) that is located in a processor (330) (p. 7, ll. 12-16). A single memory cell 370 is accessed based on the register indicator, wherein the single memory cell is allocated a storage size correlating to the bit capacity of said register (220) (p. 7, ll. 18-24). A variable width mapping process provides a correlation between the single cell variable width memory locations and the variable width register (p. 10, ll. 13-18; p. 12, ll. 12-20; p. 14, ll. 6-15). Information is transferred between the single memory cell and another component, wherein the information includes the same number of bits as the bit capacity (230) (p. 7, ll. 26-32). The bit capacity of the register is potentially varied on a per access basis to memory cells automatically, wherein all memory locations are not required to have the same width. (p. 13, ll. 14-17)

Independent claim 20 recites a variable memory width assignment method that includes analyzing a register configuration specification (410), wherein the register (331) is located in a processor (330). Bits in a portion of the register are identified, wherein said portion corresponds to information grouped in an arrangement that facilitates reduction of processing instructions (420) (p. 12, ll. 11-23). A memory location a width equal to the number of the bits in the portion of the register is assigned (430), wherein said register is arranged in accordance with a communications packet configuration specification (p. 10, l. 28 - p. 11, l. 10). The number of the bits potentially vary automatically on a per access basis to portions of the register when identifying the bits and the width potentially vary automatically

on a per access basis when assigning a single cell memory location that is equal to the number of said bits, and all memory locations are not required to have the same width (p. 13, ll. 14-17). A variable width mapping process provides a correlation between said single cell variable width memory locations and said variable width register (p. 10, ll. 13-18; p. 12, ll. 12-20; p. 14, ll. 6-15). .

Independent claim 23 recites a variable width memory assignment system that includes a means for communicating memory location identifiers 375, and a means for storing information (311) (p. 8, l. 33 – p. 9, l. 8) in uniquely identifiable different width single cell memory locations corresponding to the memory location identifiers, wherein the means for storing said information returns the number of bits equal to the width of one of the uniquely identifiable different width single cell memory locations and the width of a register (331) that is located in a processor (330) associated with the variable width memory assignment system in response to a read request. The number of bits returned by the means for storing information are potentially varied automatically per read request due to which of the uniquely identifiable different width single cell memory locations is being accessed by the read request (p. 13, ll. 14-17). A means for managing a connection (320) with the uniquely identifiable different width single cell memory locations is included, wherein the means for managing the connection supervises writing and reading of information to and from the uniquely identifiable different width single cell memory locations, wherein all memory locations are not required to have the same width, and wherein a variable width mapping process provides a correlation between the different width single cell memory locations and a variable width register (331) (p. 10, ll. 13-18; p. 12, ll. 12-20; p. 14, ll. 6-15).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1-14, 16-20 and 23-25 were properly rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent Application Publication No. 2003/0158995 to Lee et al. ("Lee") in view of U.S. Patent No. 6,230,249 to Chan et al. ("Chan").

ARGUMENT

Rejection under 35 U.S.C. §103(a) based on U.S. Patent Application Publication No. 2003/0158995 to Lee et al. ("Lee") in view of U.S. Patent No. 6,230,249 to Chan et al. ("Chan").

1. Independent claims 1, 8, 20 and 23.

To establish *prima facie* obviousness, all claim limitations must be considered. MPEP 2143.03 (citing *In re Wilson*, 424 F.2d 1382, 1385, (CCPA 1970)). Since the combination of Lee and Chan fails to disclose each element of the independent claims, the Office Action failed to establish *prima facie* obviousness.

Among other things, claims 1, 8, 20 and 23 each include "a variable width mapping process provides a correlation between said single cell variable width memory locations and said variable width register." Sections 3 and 4 of the Office Action, which set out the rejections under 35 USC 103, fail to identify a specific disclosure of a variable width mapping process that provides a correlation between said single cell variable width memory locations and said *variable width register*. Instead, citing Chan at col. 2, ll. 59-66, the Office Action states, "the variable cell size circuit must also include a register for the storing of these values.

This cited portion of Chan is as follows:

> A variable cell size circuit supports user programmable cell sizes in a memory device. The variable cell size circuit includes a counter and a comparator, and it controls successive accesses to a cell in the memory device. The comparator receives a cell size value that specifies the number of bytes for the current cell. The counter generates a count that specifies a number of accesses to the cell, and the comparator compares the count with the cell size value.

There is no specific mention of a variable width register, or of "single cell variable width memory locations receive a number of bits corresponding to the width of the single cell variable width memory locations and the width of a *variable width register*" in the cited portion.

Further, regarding Chan, section 2 (*Response to Arguments*) of the Office Action states,

> Chan et al. discloses a variable cell size circuit 200 that defines the number of bytes (number of bits that will be received in a memory location) per cell for an access operation to a cell (Col. 5, lines 2-18). Therefore, the variable cell size circuit must include a variable width register for the storage of the number of bytes, and as thus, represents the correlation between the variable width memory location and the variable width register.

Office Action at p. 2. This cited portion of Chan is as follows:

> FIG. 3 is a block diagram illustrating a variable cell size circuit to define the number of bytes per cell for an access operation to a cell. The variable cell size circuit may be used for a write or a read operation to memory. As shown in FIG. 3, the variable cell size circuit 200 includes a counter 210 and a comparator 220. The comparator 220 receives a value, entitled "cell size value", that defines the number of bytes per cell for the corresponding FIFO block. In one embodiment, the cell size value is a signal generated by the user, and it is input externally to the FIFO device 100 (FIG. 1). The counter 210 receives a clock, and for this embodiment, each clock cycle defines an access-cycle (e.g. read and write operations are executed each clock cycle). The counter 210 generates the byte address for the access operation to the current cell. The comparator 220 generates an equal "EQ" signal when the byte address is equal to the cell size value.

Both of the cited portions of Chan reproduced above do not disclose a variable width mapping process that provides a correlation between single cell variable width memory locations and a variable width register. The cited portions do not use the terms *mapping* or *register*, for example.

In fact, the cited portions of Chan appear to teach away from a mapping process that provides a correlation single cell variable width memory locations and a variable width register. Prior art references must be considered in their entirety, including portions that teach away from the claim elements. MPEP 2141.02VI.

The cited portions of Chan include, "the cell size value is a signal generated by *the user*…." (Emphasis added). Chan further teaches, "a variable cell size circuit supports *user programmable* cell sizes in a memory device." Chan at col. 1, ll. 59-60. As such, Chan teaches user-provided cell sizes, rather than using a mapping process to correlate memory locations with a register.

The Office Action fails to identify a process for correlating between single cell variable width memory locations and a variable width register explicitly taught in the reproduced portions of Chan above. Instead, the Office Action appears to allege that a

register is inherent to the Chan disclosure ("the variable cell size circuit *must* include a variable width register…"). However, MPEP 2112 notes that the Examiner must provide rationale or evidence to show inherency:

> To establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient."

(Citing *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (internal citations omitted)).

To the extent that the devices disclosed in Chan *might* include registers (though Office Action fails to provide a specific reference to this), there is no rationale or evidence provided in the Office Action that Chan teaches *variable width* registers, or a variable width mapping process that provides a correlation between single cell variable width memory locations and a variable width register. In the cited portions of Chan, Chan simply states that the variable cell size circuit receives a cell size value. There is no teaching or suggestion identified in the Office Action of a variable width register or a register configured as recited in the claims. Further, there is no disclosure of any process for correlating between single cell variable width memory locations and such a *variable width register*.

Since the combined teachings of Lee and Chan fail to disclose at least the claim elements discussed above, the Office Action failed to establish *prima facie* obviousness of claims 1, 8, 20 and 23, and the remaining claims dependent thereon.

Moreover, MPEP 2143.01 notes if a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. (citing *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)).

The Office Action proposes, "modify[ing] the system of Lee to include the variable width memory cells of Chan as well as the variable cell size circuit and further more, apply its variable memory location control method to the new variable memory cells…." Office Action at p. 4. However, Lee discloses a DRAM "with adjustable page size to raise the page hit rate." Lee at paragraph [0008]. Lee teaches a system wherein

> the DRAM types of the installed DRAM modules are identified during the computer power-up initialization (step 510). According to the respective DRAM types, the maximum page size of each DRAM module is determined and the page mask for each DRAM module is also set (step 520)

Lee at paragraph [0021]. Thus, Lee specifically discloses determining DRAM *page* size, and then goes on to disclose a particular mask structure for addresses within those DRAM pages:

> According to the invention, a 32-bit internal address, e.g., physical address, HA[31:0] can be divided into three portions: a first portion HA[31:15], a second portion HA[10:0] and a third portion HA[14:11]

Lee at paragraph [0022].

There is no indication provided in the Office Action as to how the DRAM *pages* disclosed in Lee, and the masking structure disclosed therein for the *page addresses* could be replaced by the cells and cell size circuit disclosed in Chan. It appears that the mask structure associated with DRAM pages would not apply to the variable cell sized FIFO memory cores disclosed in Chan, thus resulting in an inoperable device.

Even if the Lee device modified in the manner proposed in the Office Action could somehow operate, it would likely operate in an entirely different way, since the adjustable DRAM pages and associated DRAM controller would be replaced by the memory device and variable cell size circuit of Chan. MPEP 2143.01 notes that, if a proposed modification or combination of the prior art would change the principle of operation of the prior art disclosure being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. (Citing *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)).

For at least these reasons, Appellants believe the combination of Lee and Chan fails to establish *prima facie* obviousness of the claims.

Appellants therefore respectfully submit that the rejection of claims 1, 8, 20 and 23 under 35 U.S.C. §103(a) was improper and should be overturned.

2. Dependent claims.

The remaining claims are all ultimately dependent on one of claims 1, 8, 20 or 23, and the rejections thereof should be overturned for at least the same reasons. The dependent claims recite further elements not disclosed or suggested in Lee modified by Chan.

The Office Action states it would be obvious to modify Lee "to include the variable width memory cells of Chan as well as the variable cell size circuit and further more, apply its variable memory location control method to the *new variable memory cells*…." Office Action at p. 4 (emphasis added). Thus, the Office Action proposes replacing the DRAM pages and DRAM controller of Lee with the memory cells and variable cell size controller of Chan, resulting in "new variable memory cells."

In rejecting claims 2-7, 12, 13, 16-19, 24 and 25, the Office Action refers to the DRAM pages and DRAM controller of Lee for allegedly disclosing the elements recited in these claims. However, in the device resulting from modifying Lee based on Chan as set forth in the Office Action (with the "new variable memory cells"), these DRAM pages and DRAM controller of Lee would be replaced by the memory cells and control circuit of Chan. Therefore, the modified Lee device would not include the elements recited in the Office Action in support of the rejections of at least claims 2-7, 12, 13, 16-19, 24 and 25.

For example, claim 4 includes "each one of said plurality of single cell variable width memory locations is identified by a unique internal identifier which is referenced by said controller to access said each one of said plurality of single cell variable width memory locations." Claim 5 includes, "said controller maps said unique internal identifier to a particular external indicator."

Regarding these limitations, the Office Action states, "the memory locations of Lee in view of Chan have individual addresses (memory row address, memory column strobe)…." and cites Lee at paragraph [0019]. However, the modification of Lee proposed in the Office Action appears to replace the DRAM memory pages, and the associated memory row address and column strobe associated with a DRAM page, with the memory device of Chan. The Office Action fails to identify a unique internal identifier referenced by a controller in Chan.

Thus, the Office Action fails to identify a disclosure of each element recited in claims 12, 13, 16-19, 24 and 25, and therefore fails to establish *prima facie* obviousness.

CONCLUSION

For the above reasons, Appellants respectfully submit that the Office Action fails to establish *prima facie* obviousness of the claims. Therefore, Appellants respectfully submit that the rejections must be withdrawn, and respectfully request the Examiner be reversed and the claims be allowed.

Any inquiry regarding this Response should be directed to either Naya Chatterjee-Marathe, at Telephone No. 650.857.5781, or Mark L. Gleason at Telephone No. (612) 573-2000, Facsimile No. (612) 573-2005.

Respectfully submitted,

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Dated: 12/21/2009

/Mark L. Gleason/

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CLAIMS APPENDIX

1. A variable width memory system comprising:

a bus for communicating information;

a plurality of single cell variable width memory locations coupled to said bus, said plurality of single cell variable width memory locations store information, wherein said plurality of single cell variable width memory locations receive a number of bits corresponding to the width of the single cell variable width memory locations and the width of a variable width register that is located in a processor associated with said variable width memory system, wherein a variable width mapping process provides a correlation between said single cell variable width memory locations and said variable width register; and

a controller coupled to said bus, said controller directs access to said plurality of single cell variable width memory locations, wherein said number of bits potentially vary automatically on a per access basis depending on which single cell variable width memory location of said plurality of single cell variable width memory locations is being accessed, wherein all memory locations are not required to have the same width.

2. The variable width memory system of Claim 1 wherein said plurality of single cell variable width memory locations are included on a single memory substrate.

3. The variable width memory system of Claim 1, wherein said plurality of single cell variable width memory locations are included in a random access memory (RAM).

4. The variable width memory system of Claim 1, wherein each one of said plurality of single cell variable width memory locations is identified by a unique internal identifier which is referenced by said controller to access said each one of said plurality of single cell variable width memory locations.

5. The variable width memory system of Claim 4, wherein said controller maps said unique internal identifier to a particular external indicator, wherein components referred to by said unique internal identifier and said particular external indicator have the same bit width.

6. The variable width memory system of Claim 1, wherein the bit width of at least two of said plurality of single cell variable width memory locations is the same.

7. The variable width memory system of Claim 1, wherein the bit width of at least one of said plurality of single cell variable width memory locations is configured in accordance with criteria directed at decreasing processor operations.

8. A variable width memory mapping method comprising:

receiving a register indicator corresponding to a register that is located in a processor;

accessing a single memory cell based on said register indicator, wherein said single memory cell is allocated a storage size correlating to the bit capacity of said register, wherein a variable width mapping process provides a correlation between said single memory cell and said register;

transferring information between said single memory cell and another component, wherein said information includes the same number of bits as said bit capacity; and

potentially varying the bit capacity of said register on a per access basis to memory cells automatically, wherein all memory locations are not required to have the same width.

9. The variable width memory mapping method of Claim 8 wherein said register indicator is received from a processor.

10. The variable width memory mapping method of Claim 8 wherein said bit capacity is determined by processing criteria associated with a processor.

11. The variable width memory mapping method of Claim 8 wherein said information is part of a communication packet.

12. The variable width memory mapping method of Claim 8 wherein said information includes data associated with certain fields.

13. The variable width memory mapping method of Claim 12 wherein bits included in said data associated with certain fields are sequentially located within said memory cell.

14. The variable width memory mapping method of Claim 8 wherein a information storage system with a computer readable medium stores information in accordance with said variable width memory mapping process.

15. (Canceled)

16. The variable memory width assignment method of Claim 20 wherein said memory location is one of a plurality of memory locations of various widths.

17. The variable memory width assignment method of Claim 20 wherein said memory location has a unique identifying address.

18. The variable memory width assignment method of Claim 20 further comprises providing an association between said memory location and an external identifier.

19. The variable memory width assignment method of Claim 20 wherein said bits in said portion of said data block are arranged in a contiguous manner.

20. A variable memory width assignment method comprising:

analyzing a register configuration specification, wherein said register is located in a processor;

identifying bits in a portion of said register, wherein said portion corresponds to information grouped in an arrangement that facilitates reduction of processing instructions;

assigning a memory location a width equal to the number of said bits in said portion of said register, wherein said register is arranged in accordance with a communications packet configuration specification; and wherein the number of said bits potentially vary automatically on a per access basis to portions of said register when identifying said bits and said width potentially vary automatically on a per access basis when assigning a single cell

memory location that is equal to the number of said bits, wherein all memory locations are not required to have the same width, wherein a variable width mapping process provides a correlation between said single cell variable width memory locations and said variable width register.

21. (Canceled)

22. (Canceled)

23. A variable width memory assignment system comprising:

a means for communicating memory location identifiers; a means for storing information in uniquely identifiable different width single cell memory locations corresponding to said memory location identifiers, wherein said means for storing said information returns the number of bits equal to the width of one of said uniquely identifiable different width single cell memory locations and the width of a register that is located in a processor associated with said variable width memory assignment system in response to a read request, wherein the number of bits returned by said means for storing information are potentially varied automatically per read request due to which of said uniquely identifiable different width single cell memory locations is being accessed by said read request; and

a means for managing a connection with said uniquely identifiable different width single cell memory locations, wherein said means for managing said connection supervises writing and reading of information to and from said uniquely identifiable different width single cell memory locations, wherein all memory locations are not required to have the same width, and wherein a variable width mapping: process provides a correlation between said different width single cell memory locations and a variable width register.

24. The variable width memory assignment system of Claim 23 wherein said means for managing said connection includes a means for tracking a correspondence between said uniquely identifiable variable memory widths and register identifiers.

25. The variable width memory assignment system of Claim 24 wherein said register identifiers are provided by a means for processing said information.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.